REMARKS/ARGUMENTS

Claims 1-23 are currently pending in the present patent application, with claims 5-8 having been allowed and claims 3-4, 14-15, and 18-19 being indicated as allowable if properly rewritten in independent form in the final Office Action mailed February 13, 2009.

In Section 3 of the final Office Action, the Examiner objects to claims 1 and 5 due to informalities. The Examiner requests that Applicants rewrite the term "FFT/IFFT" in full for clarification purposes. Claims 1 and 5 have been amended as requested by the Examiner. These amendments do not change the scopes of these claims.

Under Section 10b of the Office Action the Examiner responds to the undersigned's prior arguments regarding this rejection. More specifically, the Examiner states with regard to the limitation of eliminating the need for inter-processor communication among the processing elements after the computation of the first $\log_2 P$ stages that "Figures 2-3 as the claimed invention which is clearly similar to the NPL's Figure 2." Furthermore, the Examiner states "[t]here are two ways of rejecting this limitation: (1) the Examiner equates the P=N/P as seen in section II 'Radix-2 FFT computation' in [the] right column page 513, particularly step 1, the intercommunication between processor[s] only occurs right after ($\log_2 P$)th stage; (2) the claims tried to merge all the $\log_2(N/P)$ stages into the $\log_2 P$ stages which can be reasonabl[y] interpreted as seen in Figure 2. For example[], [l]et N=16 and P=2 as seen in applicant's Figure 2, but we see no[ ]intercommunication is up to stage 3. Thus, the claimed invention either merges the first three stage[s] as [a] single stage or loosely bound the non-intercommunication between the processors or processing elements which clearly [is] saying either way in Figure 2 by Laxmi."

The Examiner appears to be confused as to what the figures, and specifically Figures 2 and 3 of the present application, illustrate regarding intercommunication between and among processing elements. While Figure 2 of Laxmi appears similar to

figures of the present application and does indeed illustrate processing elements PE and calculations performed within and among these processing elements, the figures of the present application do not illustrate what the Examiner is asserting they illustrate. This will now be explained in more detail with reference to annotated Figure 3 shown below:

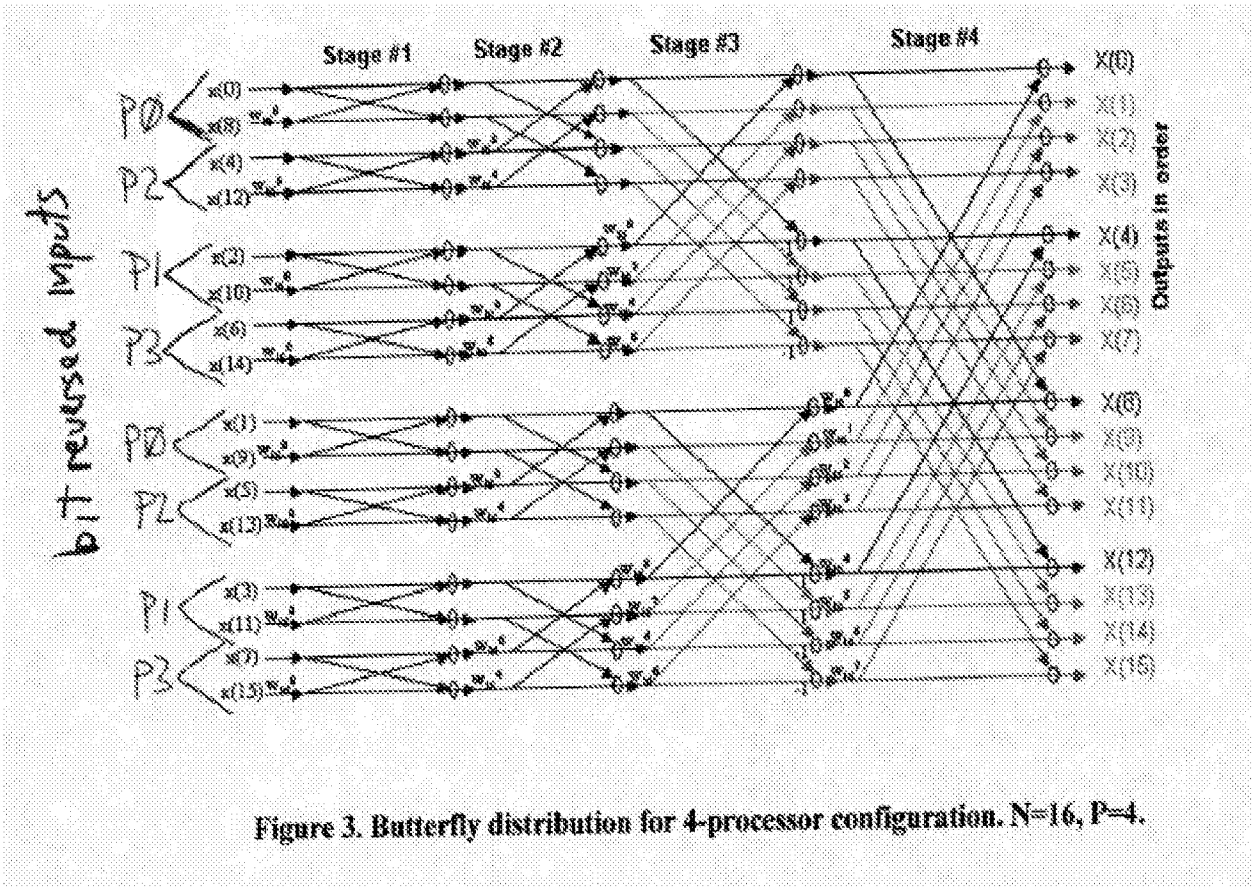
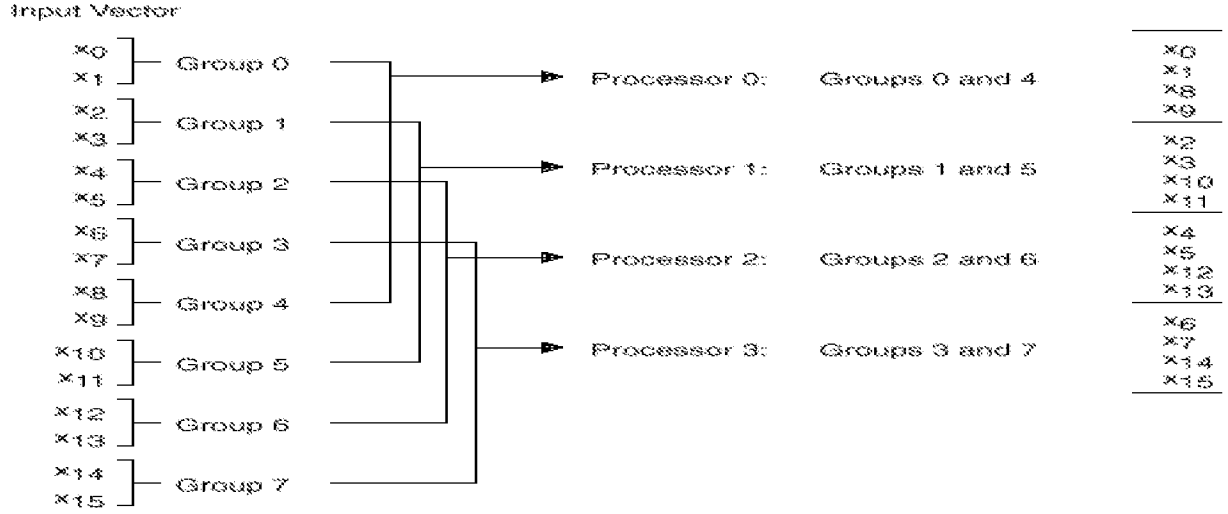


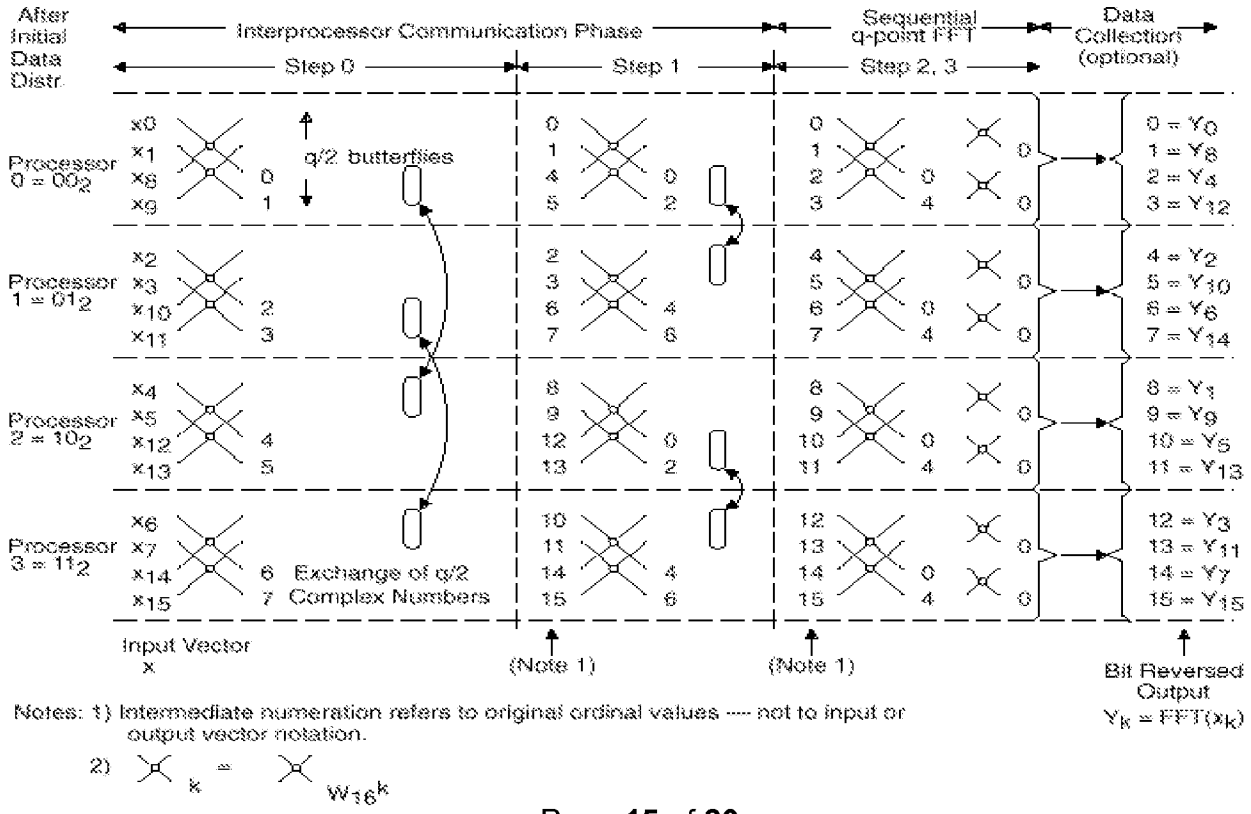
Figure 3. Butterfly distribution for 4-processor configuration. N=16, P=4.

In the annotated Figure 3 shown above, the processing elements P0-P3 associated with the sixteen inputs x(0)-x(15) are expressly labeled along the left side of the figure. Furthermore, the calculated values in the last two stages labeled 3 and 4 are color-coded to simplify understanding of the figure.

The figure below also illustrates the Butterfly distribution of the inputs for the 4-processor configuration of annotated Figure 3 shown above:



Thus, as the above figure illustrates Groups 0 and 4 are initially input to the processor P0, Groups 1 and a 5 are input to processor P1, and so on. The figure below alternatively illustrates the operation of the 4-processor configuration illustrated in annotated Figure 3 shown above:



Claim 1 recites a method for controlling processing elements in a multiprocessor architecture to provide improved throughput for FFT/IFFT computations. The method includes the steps of computing, on a multiprocessor architecture including "P" processing elements, each butterfly of the first "$\log_2 P$" stages of an FFT/IFFT on either a single one of the processing elements or on each of the "P" processing elements simultaneously. The method further includes distributing the computations of the butterflies in all the subsequent stages of the FFT/IFFT among the "P" processing elements such that each chain of cascaded butterflies consisting of those butterflies that have inputs and outputs connected together are processed by the same processing element to thereby eliminate the need for inter-processor communication among the processing elements after the computation of the first "$\log_2 P$" stages of the FFT/IFFT.

Claim 1 expressly recites that the first $\log_2 P$ stages of butterfly calculations are performed as recited and in combination with the limitation that the butterfly calculations of all subsequent stages are distributed so that inter-processor communication is eliminated for all these subsequent stage calculations. None of the prior art cited by the Examiner alone or in combination discloses or suggests these recited operations. Specifically, in Laxmi the processing elements start to communicate with each other after $\log_2 N/P$ stages (see pp. 513, right column, section II, "Radix-2 FFT Computation"), where N is the length the data sequence or number of points or samples being processed via the algorithm and P is the number of processing elements PE. Laxmi simply does not disclose eliminating communication among processing elements after $\log_2 P$ stages. In contrast, with the approach of claim 1 communications among the processing elements happens after $\log_2 P$ stages and only once for the rest of the FFT/IFFT computation as is evident from the embodiments of the invention covered by claim 1 and depicted in Figures 2 and 3 of the present application and as further illustrated in the figures presented above to assist the Examiner's understanding.

For at least these reasons, the combination of elements recited in claim 1 is allowable. Dependent claims 2-4 are allowable for at least the same reasons as claim 1 and due to the additional limitations added by each of these dependent claims.

Independent claim 9 recites a method of performing a fast Fourier transform or inverse fast Fourier transform on an input signal. The method includes storing samples of the input signal in a memory, retrieving the samples from the memory and from these retrieved samples calculating the butterfly computational blocks for the first $\log_2 P$ stages of the transform on a single processor or on a plurality of processors operating in parallel. The method further includes eliminating the need for communication among and between the processors after the computation of the first "$\log_2 P$" stages of the transform by calculating chains of butterfly computational blocks corresponding to the subsequent stages of the transform within each of the processors, each chain of butterfly computational blocks that is calculated in a respective processor having inputs and outputs coupled in series.

Once again, as discussed above with reference to claim 1, Laxmi neither discloses nor suggests calculating butterfly computational blocks for the first $\log_2 P$ stages of the transform on a single processor or on a plurality of processors operating in parallel and eliminating the need for communication among and between the processors after the computation of the first "$\log_2 P$" stages. In contrast, with the approach of Laxmi the processing elements start to communicate with each other after $\log_2 N/P$ stages.

For at least these reasons, the combination of elements recited in claim 9 is allowable. Dependent claims 10-15 are allowable for at least the same reasons as claim 9 and due to the additional limitations added by each of these dependent claims.

Independent claim 16 recites a processor system including a memory operable to store samples of an input signal and a plurality of processors coupled to the memory. The plurality of processors are operable to receive the samples from the memory and to use the samples to execute the butterfly computational blocks for the

first "$\log_2 P$" stages of a fast Fourier transform or inverse fast Fourier transform on either a single one of the processors or on a plurality of the processors operating in parallel. Address circuitry is coupled to the memory and processor and operable to distribute the computation of the butterfly computational blocks in all stages subsequent to the first $\log_2 P$ stages among the plurality of processors such that each chain of cascaded butterfly computational blocks in the transform are coupled in series and are computed by the same processor to thereby eliminate the need for communication among and between the processors after the computation of the first "$\log_2 P$" stages of the transform.

Laxmi neither discloses nor suggests a plurality of processors that execute the butterfly computational blocks for the first "$\log_2 P$" stages of a fast Fourier transform or inverse fast Fourier transform on either a single one of the processors or on a plurality of the processors operating in parallel and address circuitry that distributes the computation of the butterfly computational blocks in all stages subsequent to the first $\log_2 P$ stages among the plurality of processors such that each chain of cascaded butterfly computational blocks in the transform are coupled in series and are computed by the same processor. This eliminates the need for communication among and between the processors after the computation of the first "$\log_2 P$" stages of the transform.. In contrast, as already discussed above, with the approach of Laxmi the processing elements start to communicate with each other after $\log_2 N/P$ stages.

For at least these reasons, the combination of elements recited in claim 16 is allowable. Dependent claims 17-20 are allowable for at least the same reasons as claim 16 and due to the additional limitations added by each of these dependent claims.

Independent claim 21 is allowable for reasons similar to those discussed with reference to claim 16 and dependent claims 22-23 are allowable for at least the same reasons as claim 21 and due to the additional limitations added by each of these dependent claims.

In Sections 7 and 8 the Examiner maintains his rejections of claims 11-13 under 35 U.S.C. § 103(a) as being unpatentable over Laxmi. As discussed above with regard to independent claim 9, dependent claims 11-13 are allowable for at least the same reasons as independent claim 9 from which each of these dependent claims ultimately depends.

Independent claim 5 is allowable for reasons similar to those discussed above with regard to independent claim 16. Furthermore, the Examiner has not shown that the art of record teaches or suggest, in combination with the other elements of claim 5, the elements of means for counting and means for computing twiddle factors for the butterfly computations at each processing elements, the means for computing initializing the means for counting and then incrementing the means for counting by a value corresponding to the number of processing elements "P" and appending the result with a specified number of "0"s.

For at least these reasons, the combination of elements recited in independent claim 5 is allowable. Dependent claims 6-8 are allowable for at least the same reasons as claim 5 and due to the additional limitations added by each of these dependent claims.

For these reasons, the combination of elements recited in claim 1 is allowable and the remaining independent claims are allowable for reasons similar to claim 1. All dependent claims are allowable for at least the same reasons as the associated independent claim and due to the additional limitations added by each of these dependent claims.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. **Should the Examiner have any further questions about the application, Applicants respectfully request the Examiner to contact the undersigned attorney at (425) 455-5575 to arrange for a telephone interview to discuss the outstanding issues.** If the need for any fee in addition to any fee paid with this response is found, for any

reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON LLP

/Paul F. Rusyn/

Paul F. Rusyn
Registration No. 42,118
Attorney for Applicants
155 – 108th Avenue NE, Suite 350
Bellevue, WA 98004-5973
(425) 455-5575 Phone
(425) 455-5575 Fax